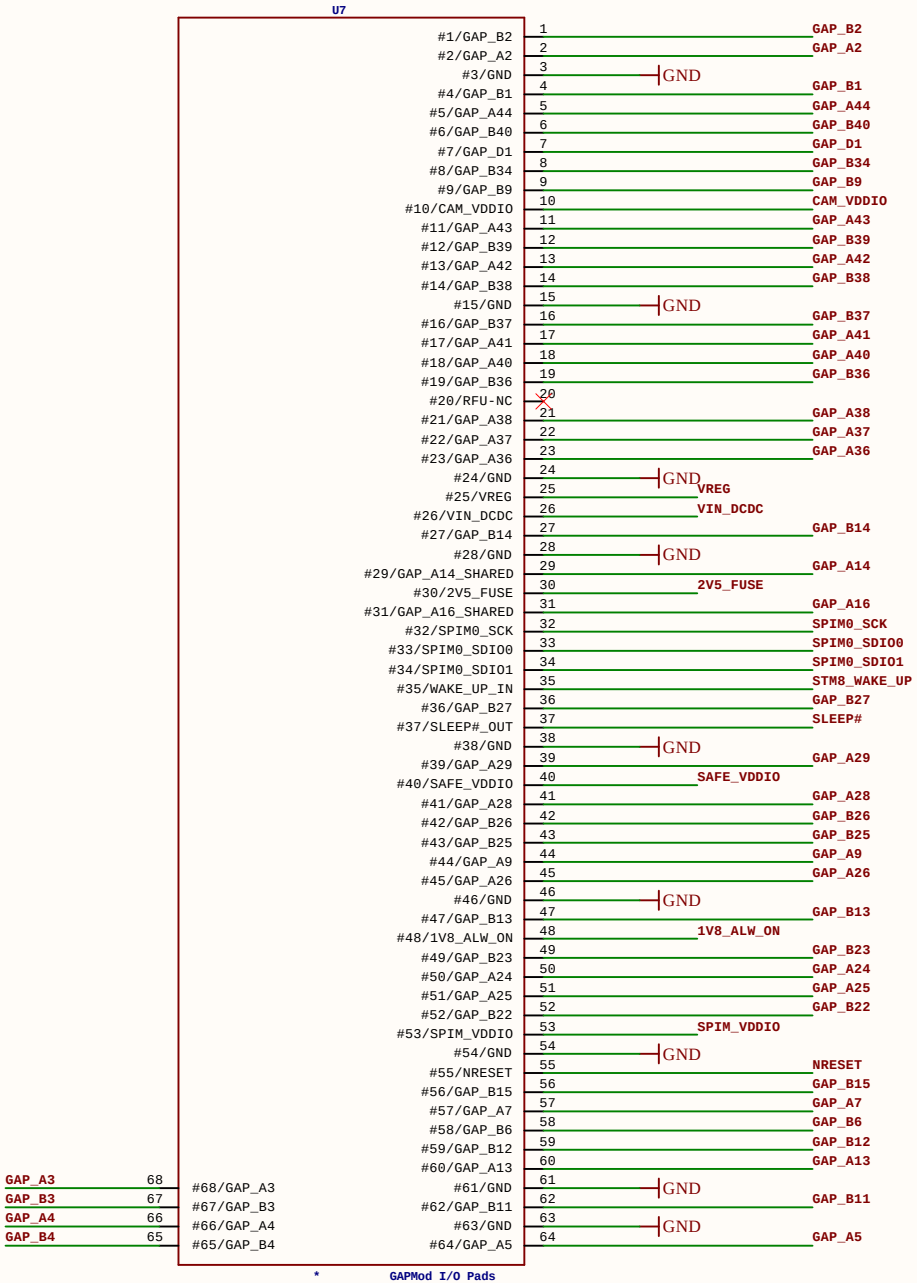
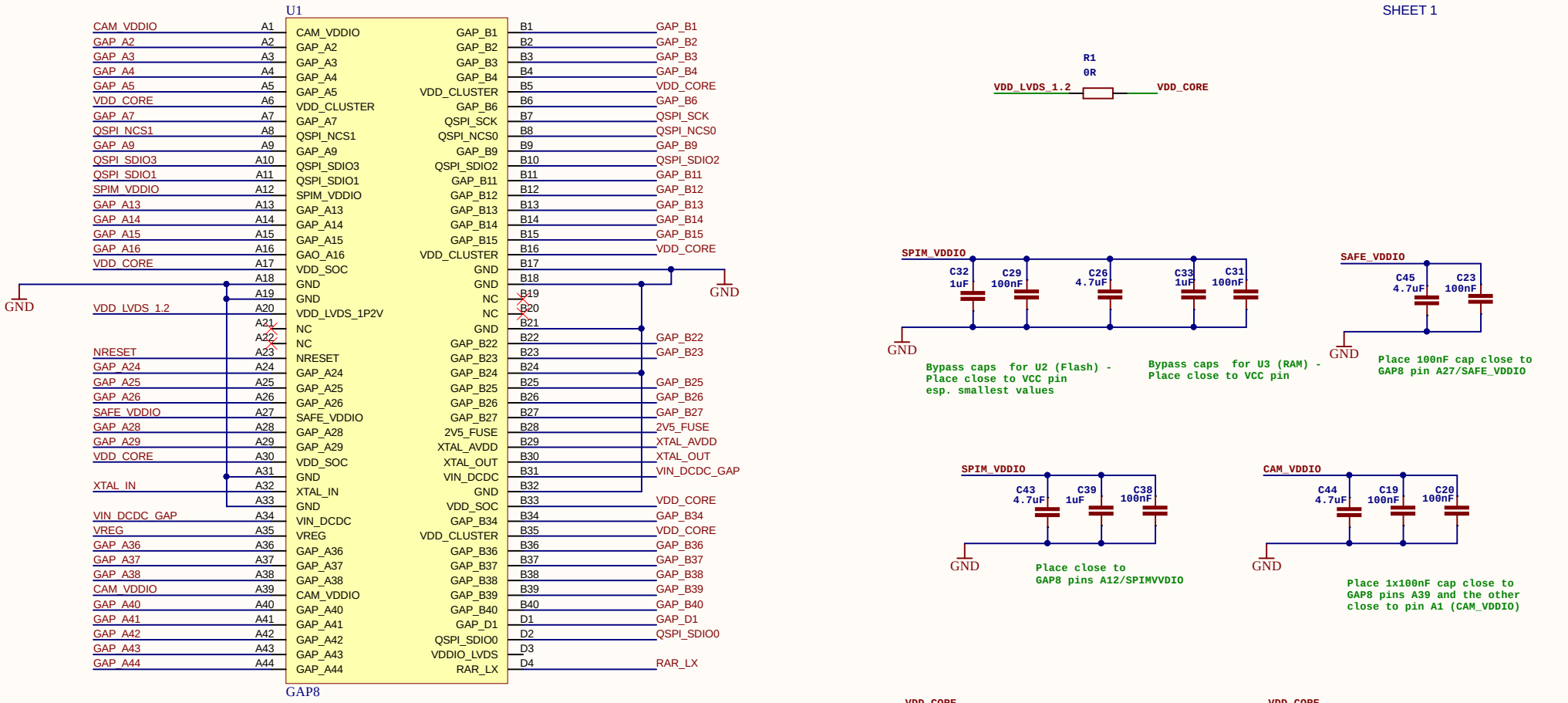
SHEET 0



Title	GAPMod	
Size A4	Number Sheet 0	Revision
Date: 07/07/2020		Sheet of
File: C:\Users\..\S0_Gapmod.SchDoc		Drawn By:


U1
CAM_VDDIO A1
GAP_A2 A2
GAP_A3 A3
GAP_A4 A4
GAP_A5 A5
VDD_CORE A6
GAP_A7 A7
QSPI_NCS1 A8
GAP_A9 A9
QSPI_SDIO3 A10
QSPI_SDIO1 A11
SPIM_VDDIO A12
GAP_A13 A13
GAP_A14 A14
GAP_A15 A15
GAP_A16 A16
VDD_CORE A17
A18
A19
VDD_LVDS_1.2 A20
A21
A22
NRESET A23
GAP_A24 A24
GAP_A25 A25
GAP_A26 A26
SAFE_VDDIO A27
GAP_A28 A28
GAP_A29 A29
VDD_CORE A30
A31
XTAL_IN A32
A33
VIN_DCDC_GAP A34
VREG A35
GAP_A36 A36
GAP_A37 A37
GAP_A38 A38
CAM_VDDIO A39
GAP_A40 A40
GAP_A41 A41
GAP_A42 A42
GAP_A43 A43
GAP_A44 A44
CAM_VDDIO
GAP_A2
GAP_A3
GAP_A4
GAP_A5
VDD_CLUSTER
GAP_A7
QSPI_NCS1
GAP_A9
QSPI_SDIO3
QSPI_SDIO1
GAP_A13
GAP_A14
GAP_A15
GAO_A16
VDD_SOC
GND
GND
VDD_LVDS_1P2V
NC
NC
NRESET
GAP_A24
GAP_A25
GAP_A26
SAFE_VDDIO
GAP_A28
GAP_A29
VDD_SOC
GND
XTAL_IN
GND
VIN_DCDC
VREG
GAP_A36
GAP_A37
GAP_A38
CAM_VDDIO
GAP_A40
GAP_A41
GAP_A42
GAP_A43
GAP_A44
GAP_B1 B1
GAP_B2 B2
GAP_B3 B3
GAP_B4 B4
VDD_CLUSTER B5
GAP_B6 B6
QSPI_SCK B7
QSPI_NCS0 B8
GAP_B9 B9
QSPI_SDIO2 B10
GAP_B11 B11
GAP_B12 B12
GAP_B13 B13
GAP_B14 B14
GAP_B15 B15
VDD_CLUSTER B16
GND B17
GND B18
NC B19
NC B20
GND B21
GAP_B22 B22
GAP_B23 B24
GAP_B24 B25
GAP_B25 B26
GAP_B26 B27
GAP_B27 B28
2V5_FUSE B29
XTAL_AVDD B30
XTAL_OUT B31
VIN_DCDC B32
GND B33
VDD_SOC B34
GAP_B34 B35
VDD_CLUSTER B36
GAP_B36 B37
GAP_B37 B38
GAP_B38 B39
GAP_B39 B40
GAP_B40 D1
GAP_D1 D2
QSPI_SDIO0 D3
VDDIO_LVDS D4
RAR_LX
GAP_B1
GAP_B2
GAP_B3
GAP_B4
VDD_CORE
GAP_B6
QSPI_SCK
QSPI_NCS0
GAP_B9
QSPI_SDIO2
GAP_B11
GAP_B12
GAP_B13
GAP_B14
GAP_B15
VDD_CORE
GAP_B22
GAP_B23
GAP_B25
GAP_B26
GAP_B27
2V5_FUSE
XTAL_AVDD
XTAL_OUT
VIN_DCDC_GAP
VDD_CORE
GAP_B34
VDD_CORE
GAP_B36
GAP_B37
GAP_B38
GAP_B39
GAP_B40
GAP_D1
QSPI_SDIO0
RAR_LX
GND
GND
GAP8
SHEET 1
R1
0R
VDD_LVDS_1.2
VDD_CORE
SPIM_VDDIO
C32 1uF
C29 100nF
C26 4.7uF
C33 1uF
C31 100nF
GND
Bypass caps for U2 (Flash) - Place close to VCC pin esp. smallest values
Bypass caps for U3 (RAM) - Place close to VCC pin
SAFE_VDDIO
C45 4.7uF
C23 100nF
GND
Place 100nF cap close to GAP8 pin A27/SAFE_VDDIO
SPIM_VDDIO
C43 4.7uF
C39 1uF
C38 100nF
GND
Place close to GAP8 pins A12/SPIMVVDIO
CAM_VDDIO
C44 4.7uF
C19 100nF
C20 100nF
GND
Place 1x100nF cap close to GAP8 pins A39 and the other close to pin A1 (CAM_VDDIO)
VDD_CORE
C10 1uF
C12 100nF
C13 100nF
C14 100nF
GND
Place 100nF caps close to GAP8 pins "VDD_CLUSTER"
VDD_CORE
C6 1uF
C7 100nF
C8 100nF
C9 100nF
GND
Place 100nF caps close to GAP8 pins "VDD_SOC"
Title GAP8 & supply
Size A4
Number Sheet 1
Revision
Date: 07/07/2020
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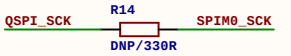
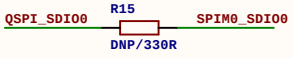
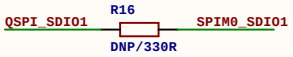
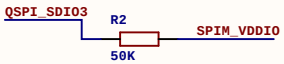
File: C:\Users\..\S1_GAP8.SchDoc
Drawn By:

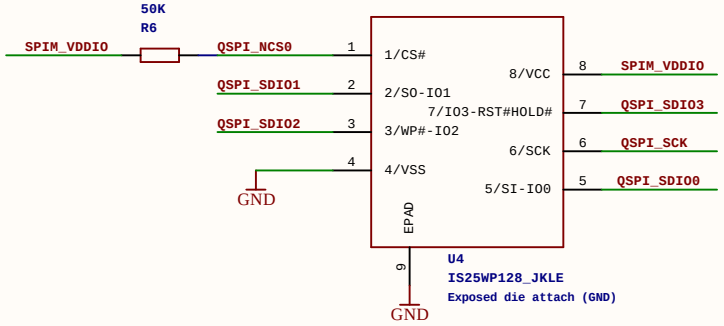




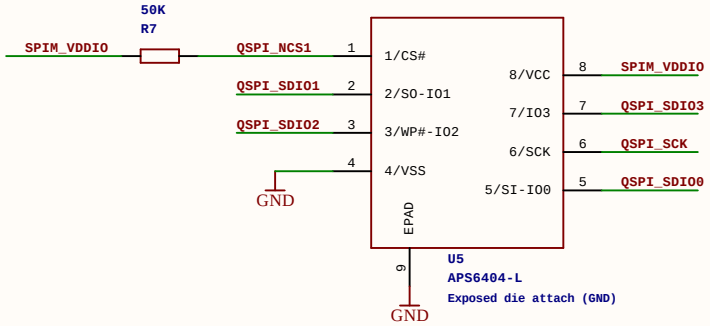




NB : Pin IO3 of Flash memory is hold# at power up.
So need to be seen at logic '1' to start up properly



FLASH

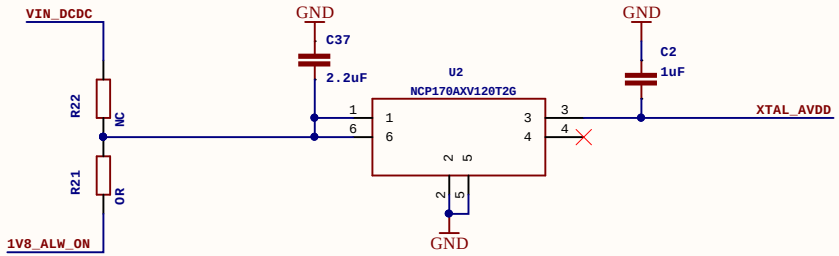


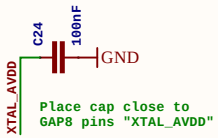
RAM

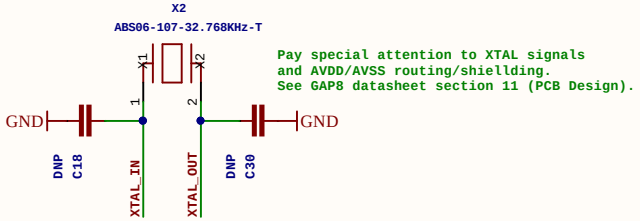
RAM and Flash get QPI bus direct from GAP8;
SCK and SDIO0-1 are also routed to GAPMod pads through series R.

Title	OCTOSPI memories	
Size A4	Number Sheet 2	Revision
Date: 07/07/2020		Sheet of
File: C:\Users\..\S2_QSPIMemories.SchDoc		Drawn By:

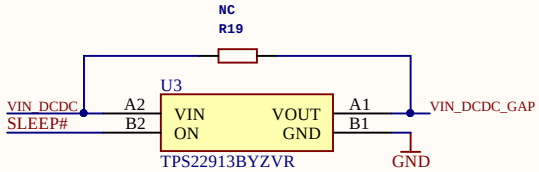
32KHz CRSYTAL SECTION

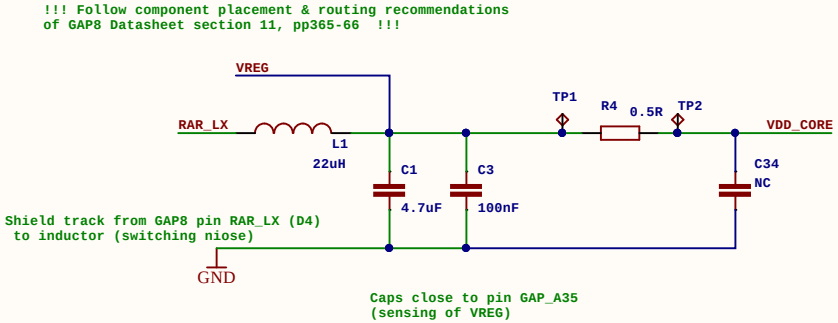


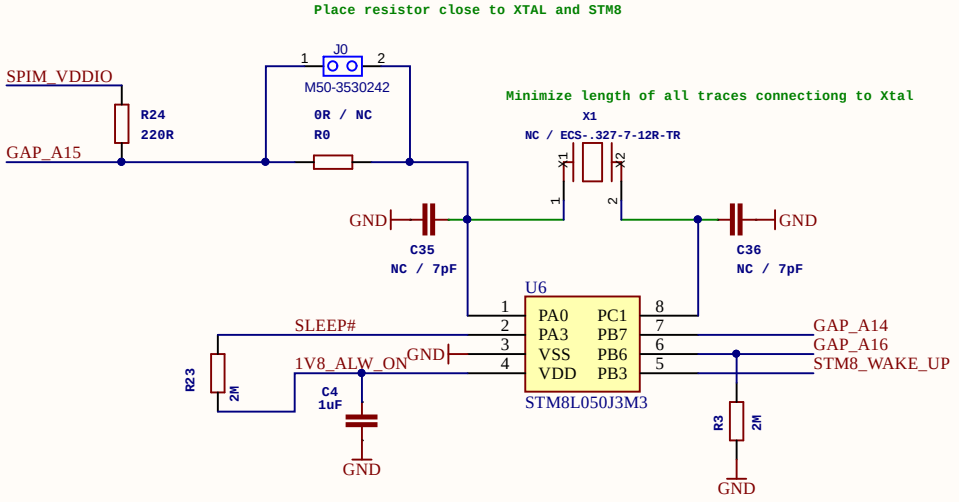




GAP8 CORE POWER MANAGEMENT







Title XTAL & SLEEP		
Size A4	Number Sheet 3	Revision
Date: 07/07/2020		Sheet of
File: C:\Users\..\S3_Xtal.SchDoc		Drawn By: