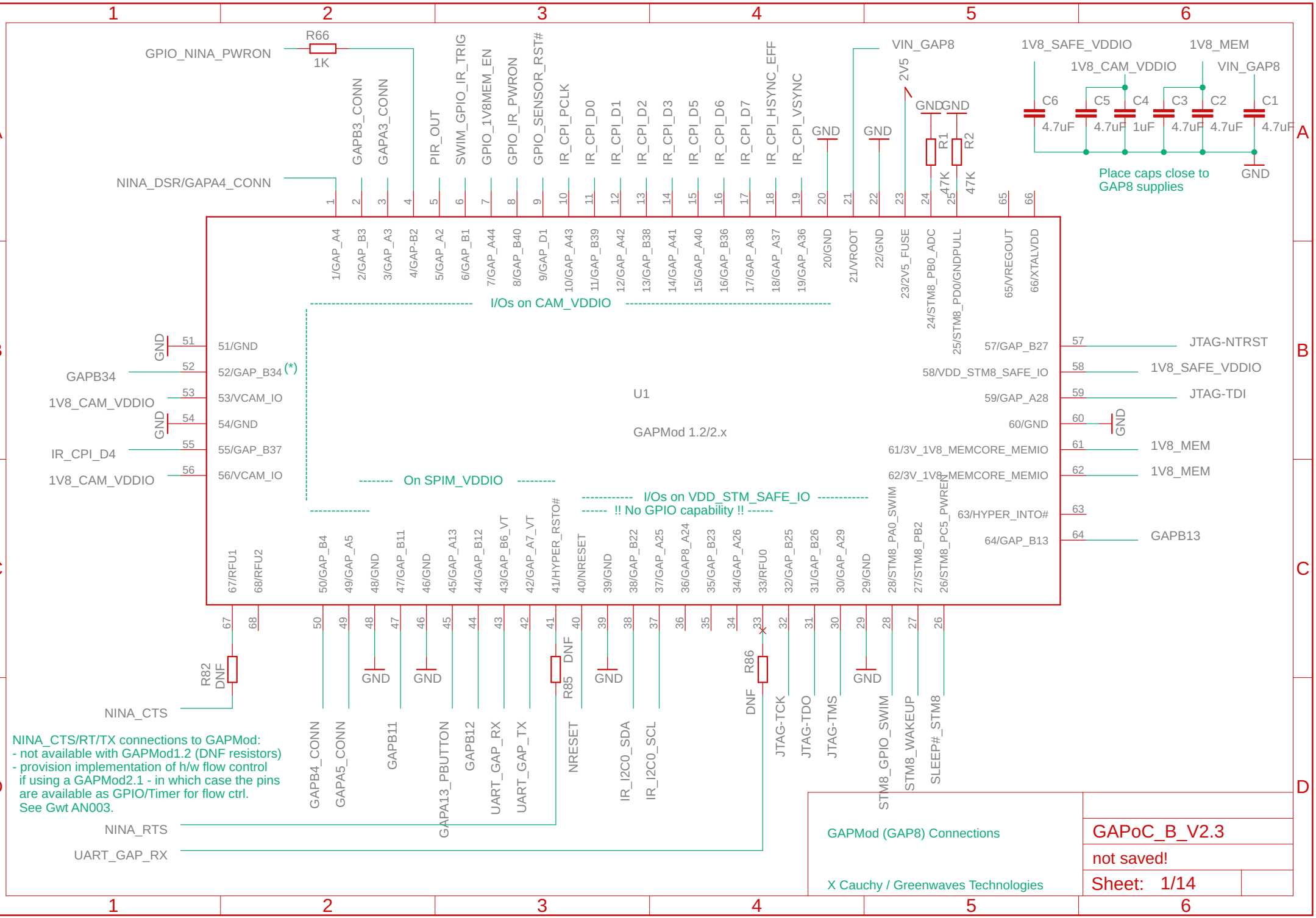
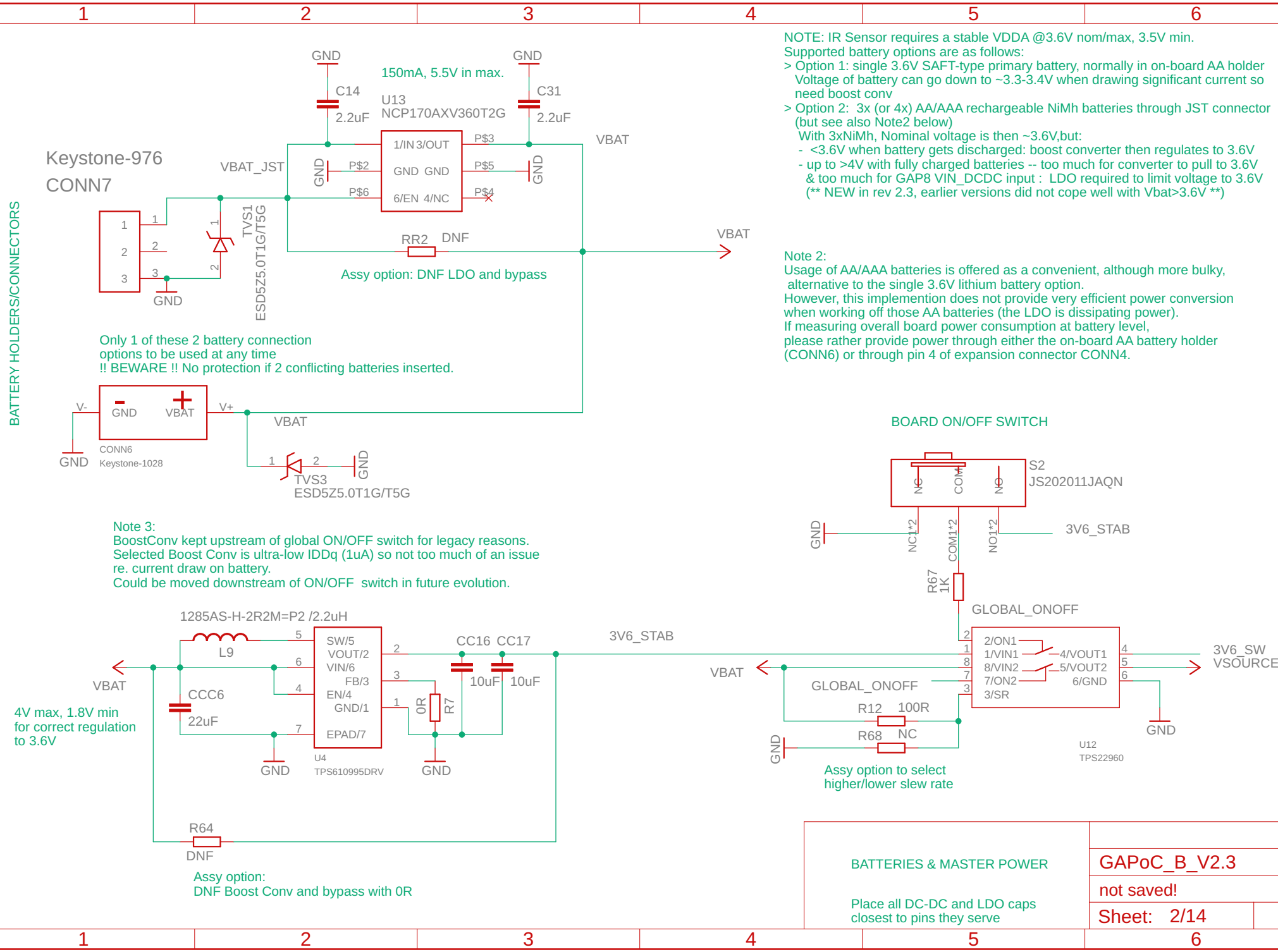
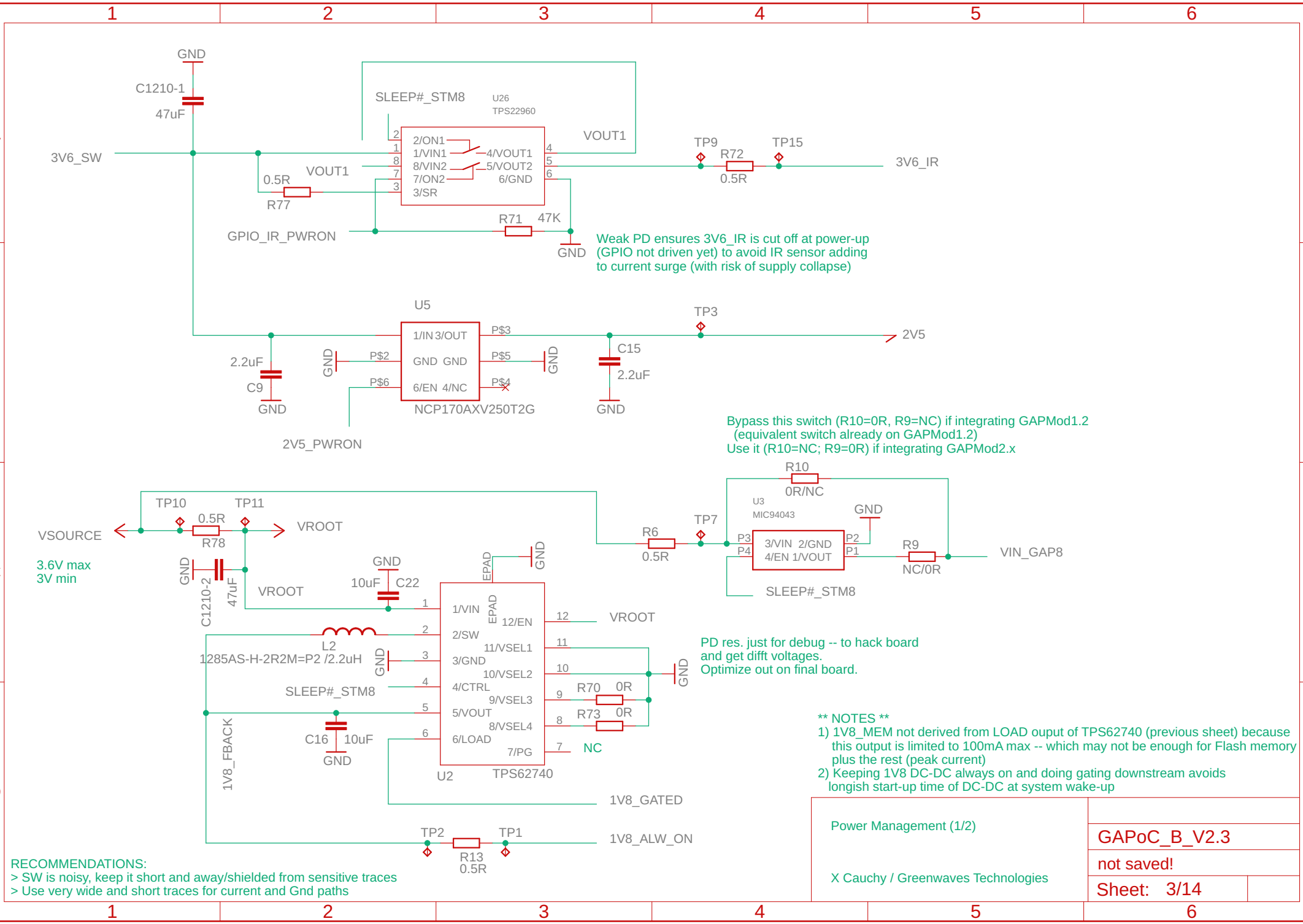
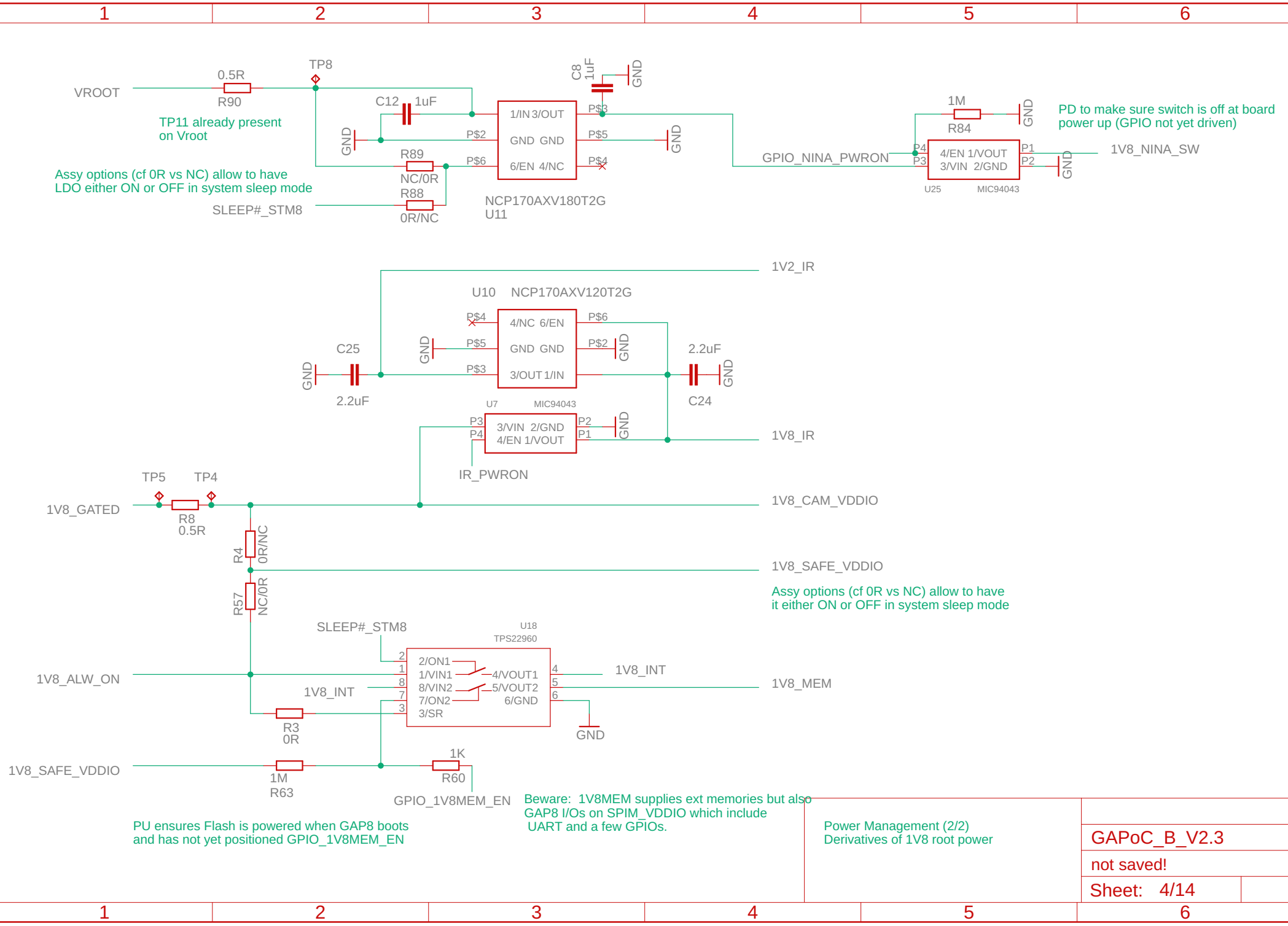

GPIO_NINA_PWRON
R66
1K
NINA_DSR/GAPA4_CONN
GAPB3_CONN
GAPA3_CONN
PIR_OUT
SWIM_GPIO_IR_TRIG
GPIO_1V8MEM_EN
GPIO_IR_PWRON
GPIO_SENSOR_RST#
IR_CPI_PCLK
IR_CPI_D0
IR_CPI_D1
IR_CPI_D2
IR_CPI_D3
IR_CPI_D5
IR_CPI_D6
IR_CPI_D7
IR_CPI_HSYNC_EFF
IR_CPI_VSYNC
GND
VIN_GAP8
2V5
R1
R2
47K
1V8_SAFE_VDDIO
1V8_MEM
1V8_CAM_VDDIO
C6
C5
C4
C3
C2
C1
4.7uF
1uF
Place caps close to GAP8 supplies
1/GAP_A4
2/GAP_B3
3/GAP_A3
4/GAP-B2
5/GAP_A2
6/GAP_B1
7/GAP_A44
8/GAP_B40
9/GAP_D1
10/GAP_A43
11/GAP_B39
12/GAP_A42
13/GAP_B38
14/GAP_A41
15/GAP_A40
16/GAP_B36
17/GAP_A38
18/GAP_A37
19/GAP_A36
20/GND
21/VROOT
22/GND
23/2V5_FUSE
24/STM8_PB0_ADC
25/STM8_PD0/GNDPULL
65/VREGOUT
66/XTALVDD
I/Os on CAM_VDDIO
U1
GAPMod 1.2/2.x
51/GND
52/GAP_B34 (*)
53/VCAM_IO
54/GND
55/GAP_B37
56/VCAM_IO
GAPB34
IR_CPI_D4
57/GAP_B27
58/VDD_STM8_SAFE_IO
59/GAP_A28
60/GND
61/3V_1V8_MEMCORE_MEMIO
62/3V_1V8_MEMCORE_MEMIO
63/HYPER_INTO#
64/GAP_B13
JTAG-NTRST
JTAG-TDI
1V8_MEM
GAPB13
On SPIM_VDDIO
I/Os on VDD_STM_SAFE_IO
!! No GPIO capability !!
67/RFU1
68/RFU2
50/GAP_B4
49/GAP_A5
48/GND
47/GAP_B11
46/GND
45/GAP_A13
44/GAP_B12
43/GAP_B6_VT
42/GAP_A7_VT
41/HYPER_RSTO#
40/NRESET
39/GND
38/GAP_B22
37/GAP_A25
36/GAP8_A24
35/GAP_B23
34/GAP_A26
33/RFU0
32/GAP_B25
31/GAP_B26
30/GAP_A29
29/GND
28/STM8_PA0_SWIM
27/STM8_PB2
26/STM8_PC5_PWREQ
R82
DNF
R85
R86
NINA_CTS
NINA_RTS
UART_GAP_RX
GAPB4_CONN
GAPA5_CONN
GAPB11
GAPA13_PBUTTON
GAPB12
UART_GAP_RX
UART_GAP_TX
NRESET
IR_I2C0_SDA
IR_I2C0_SCL
JTAG-TCK
JTAG-TDO
JTAG-TMS
STM8_GPIO_SWIM
STM8_WAKEUP
SLEEP#_STM8
NINA_CTS/RT/TX connections to GAPMod:
- not available with GAPMod1.2 (DNF resistors)
- provision implementation of h/w flow control if using a GAPMod2.1 - in which case the pins are available as GPIO/Timer for flow ctrl. See Gwt AN003.
GAPMod (GAP8) Connections
X Cauchy / Greenwaves Technologies
GAPoC_B_V2.3
not saved!
Sheet: 1/14


BATTERY HOLDERS/CONNECTORS
Keystone-976
CONN7
VBAT_JST
GND
TVS1
ESD5Z5.0T1G/T5G
RR2 DNF
VBAT
Assy option: DNF LDO and bypass
Only 1 of these 2 battery connection
options to be used at any time
!! BEWARE !! No protection if 2 conflicting batteries inserted.
V-
V+
CONN6
Keystone-1028
TVS3
ESD5Z5.0T1G/T5G
150mA, 5.5V in max.
C14
2.2uF
U13
NCP170AXV360T2G
C31
2.2uF
1/IN 3/OUT
GND GND
6/EN 4/NC
P$2
P$3
P$4
P$5
P$6
NOTE: IR Sensor requires a stable VDDA @3.6V nom/max, 3.5V min.
Supported battery options are as follows:
> Option 1: single 3.6V SAFT-type primary battery, normally in on-board AA holder
Voltage of battery can go down to ~3.3-3.4V when drawing significant current so
need boost conv
> Option 2: 3x (or 4x) AA/AAA rechargeable NiMh batteries through JST connector
(but see also Note2 below)
With 3xNiMh, Nominal voltage is then ~3.6V,but:
- <3.6V when battery gets discharged: boost converter then regulates to 3.6V
- up to >4V with fully charged batteries -- too much for converter to pull to 3.6V
& too much for GAP8 VIN_DCDC input : LDO required to limit voltage to 3.6V
(** NEW in rev 2.3, earlier versions did not cope well with Vbat>3.6V **)
Note 2:
Usage of AA/AAA batteries is offered as a convenient, although more bulky,
alternative to the single 3.6V lithium battery option.
However, this implemention does not provide very efficient power conversion
when working off those AA batteries (the LDO is dissipating power).
If measuring overall board power consumption at battery level,
please rather provide power through either the on-board AA battery holder
(CONN6) or through pin 4 of expansion connector CONN4.
BOARD ON/OFF SWITCH
S2
JS202011JAQN
NC
COM
NO
NC1*2
COM1*2
NO1*2
3V6_STAB
R67
1K
GLOBAL_ONOFF
Note 3:
BoostConv kept upstream of global ON/OFF switch for legacy reasons.
Selected Boost Conv is ultra-low IDDq (1uA) so not too much of an issue
re. current draw on battery.
Could be moved downstream of ON/OFF switch in future evolution.
1285AS-H-2R2M=P2 /2.2uH
L9
SW/5
VOUT/2
VIN/6
FB/3
EN/4
GND/1
EPAD/7
U4
TPS610995DRV
CCC6
22uF
CC16 CC17
10uF
10uF
0R
R7
3V6_STAB
4V max, 1.8V min
for correct regulation
to 3.6V
2/ON1
1/VIN1
8/VIN2
7/ON2
3/SR
4/VOUT1
5/VOUT2
6/GND
3V6_SW
VSOURCE
U12
TPS22960
R12 100R
R68 NC
Assy option to select
higher/lower slew rate
R64
DNF
Assy option:
DNF Boost Conv and bypass with 0R
BATTERIES & MASTER POWER
Place all DC-DC and LDO caps
closest to pins they serve
GAPoC_B_V2.3
not saved!
Sheet: 2/14


GND
C1210-1
47uF
3V6_SW
SLEEP#_STM8
U26
TPS22960
2/ON1
1/VIN1
8/VIN2
7/ON2
3/SR
4/VOUT1
5/VOUT2
6/GND
VOUT1
0.5R
R77
GPIO_IR_PWRON
R71
47K
GND
TP9
R72
TP15
0.5R
3V6_IR
Weak PD ensures 3V6_IR is cut off at power-up
(GPIO not driven yet) to avoid IR sensor adding
to current surge (with risk of supply collapse)
U5
1/IN 3/OUT
GND GND
6/EN 4/NC
P$3
P$2
P$5
P$6
P$4
NCP170AXV250T2G
2.2uF
C9
GND
C15
2.2uF
TP3
2V5
2V5_PWRON
Bypass this switch (R10=0R, R9=NC) if integrating GAPMod1.2
(equivalent switch already on GAPMod1.2)
Use it (R10=NC; R9=0R) if integrating GAPMod2.x
R10
0R/NC
U3
MIC94043
3/VIN 2/GND
4/EN 1/VOUT
P3
P4
P2
P1
R6
0.5R
TP7
R9
NC/0R
VIN_GAP8
SLEEP#_STM8
TP10
TP11
0.5R
R78
VSOURCE
VROOT
3.6V max
3V min
C1210-2
47uF
10uF
C22
EPAD
1/VIN
2/SW
3/GND
4/CTRL
5/VOUT
6/LOAD
12/EN
11/VSEL1
10/VSEL2
9/VSEL3
8/VSEL4
7/PG
L2
1285AS-H-2R2M=P2 /2.2uH
SLEEP#_STM8
C16
10uF
1V8_FBACK
U2
TPS62740
R70
R73
0R
NC
1V8_GATED
PD res. just for debug -- to hack board
and get difft voltages.
Optimize out on final board.
TP2
TP1
R13
0.5R
1V8_ALW_ON
** NOTES **
1) 1V8_MEM not derived from LOAD ouput of TPS62740 (previous sheet) because
this output is limited to 100mA max -- which may not be enough for Flash memory
plus the rest (peak current)
2) Keeping 1V8 DC-DC always on and doing gating downstream avoids
longish start-up time of DC-DC at system wake-up
RECOMMENDATIONS:
> SW is noisy, keep it short and away/shielded from sensitive traces
> Use very wide and short traces for current and Gnd paths
Power Management (1/2)
X Cauchy / Greenwaves Technologies
GAPoC_B_V2.3
not saved!
Sheet: 3/14


VROOT
0.5R
R90
TP8
TP11 already present on Vroot
C12 1uF
GND
R89
NC/0R
R88
0R/NC
SLEEP#_STM8
Assy options (cf 0R vs NC) allow to have LDO either ON or OFF in system sleep mode
C8 1uF
1/IN 3/OUT
GND GND
6/EN 4/NC
P$1
P$2
P$3
P$4
P$5
P$6
NCP170AXV180T2G
U11
GPIO_NINA_PWRON
1M
R84
4/EN 1/VOUT
3/VIN 2/GND
U25
MIC94043
PD to make sure switch is off at board power up (GPIO not yet driven)
1V8_NINA_SW
1V2_IR
U10 NCP170AXV120T2G
4/NC 6/EN
C25
2.2uF
C24
U7 MIC94043
3/VIN 2/GND
4/EN 1/VOUT
IR_PWRON
1V8_IR
TP5
TP4
1V8_GATED
R8
0.5R
R4
0R/NC
R57
NC/0R
1V8_CAM_VDDIO
1V8_SAFE_VDDIO
Assy options (cf 0R vs NC) allow to have it either ON or OFF in system sleep mode
U18
TPS22960
2/ON1
1/VIN1
8/VIN2
7/ON2
3/SR
4/VOUT1
5/VOUT2
6/GND
1V8_ALW_ON
1V8_INT
1V8_MEM
R3
0R
1V8_SAFE_VDDIO
1M
R63
1K
R60
GPIO_1V8MEM_EN
PU ensures Flash is powered when GAP8 boots and has not yet positioned GPIO_1V8MEM_EN
Beware: 1V8MEM supplies ext memories but also GAP8 I/Os on SPIM_VDDIO which include UART and a few GPIOs.
Power Management (2/2)
Derivatives of 1V8 root power
GAPoC_B_V2.3
not saved!
Sheet: 4/14

NOTE on LEDs :
I/Os controlling LEDs are 0V-1V8 while Vf of LED is ~1.8v-2V.
In this design, applying 2.5V on anode and controlling cathode from I/O, so that:
- LED ON when I/Os is 0V.
- LED Off when I/O driven to either Logic1 (1.8V) or (better) High-Z
Some small current might still circulate in OFF mode,
but not enough to light LED (or perhaps, if applying 1 Logic1 rather than High-Z, extremely dim).
Not an issue from power perspective as only used in debug mode
(2V5 can be switched off in normal mode)
[Also applies to other 2V5-powered LEDs used in this design]

Using difft LED color scheme vs. Nina spec

Biased for I~2mA

LED2
A_R
Red
A_YG
K_R
K_YG
Y-Gn
SML-D22MUW
R21 330R
R22 330R
LED_R
GND
LED_G always on if LEDs enabled

Switchable 2V5 (cf DIP Switch)
Turn on for debug/bring-up,
off to save power

2V5_LED

LED1
APHD1608LCGCK
R23 330R
LED_SINGLE

NB - Nina will driving I/O to Logic1=1.8V will mean LED off.
At this point stil 2.5-1.8=0.7V across LED --
not strictly off but not sufficient for LED to shine

NB - Allowing control of GPIO_NINA_PWRON
from here to force enable of
NINA's VDD when programming thru SWD

1V8_NINA_SW
SWCLK
SWDIO
GPIO_NINA_PWRON
NINA_RST#
GND
CONN2
TC2030-IDC-NL Footprint

UART_TO_NINA
UART_FROM_NINA
NINA_CTS
R11 47K GND
GND GND

30 GND
29 29/NFC2
28 28/NFC1
27 IO_27
26 GND
25 IO_25
24 IO_24
23 23/UART_RXD
22 22/UART_TXD
21 21/UART_CTS

LED_R
1 1/RED
2 IO_2
3 IO_3
4 IO_4
5 IO_5
GND
6 GND
NINA_SW1/2
7 7/GREEN/SW1
LED_SINGLE
8 8/BLUE
9 9/VCC_IO
1V8_NINA_SW
10 10/VCC

20 20/UART_RTS NINA_RTS
(internal PU)
19 19/RESET_N NINA_RST#
R103 0R
18 18/SW2 NINA_SW1/2
R24 0R
17 17/UART_DSR NINA_DSR/GAPA4_CONN
16 16/UART_DTR
NC R32
15 15/SWDIO SWDIO
14 GND GND
13 13/ANT(NC)
12 GND GND
11 11/SWCLK SWCLK

C17 4.7uF
C18 1uF
C19 100nF
GND

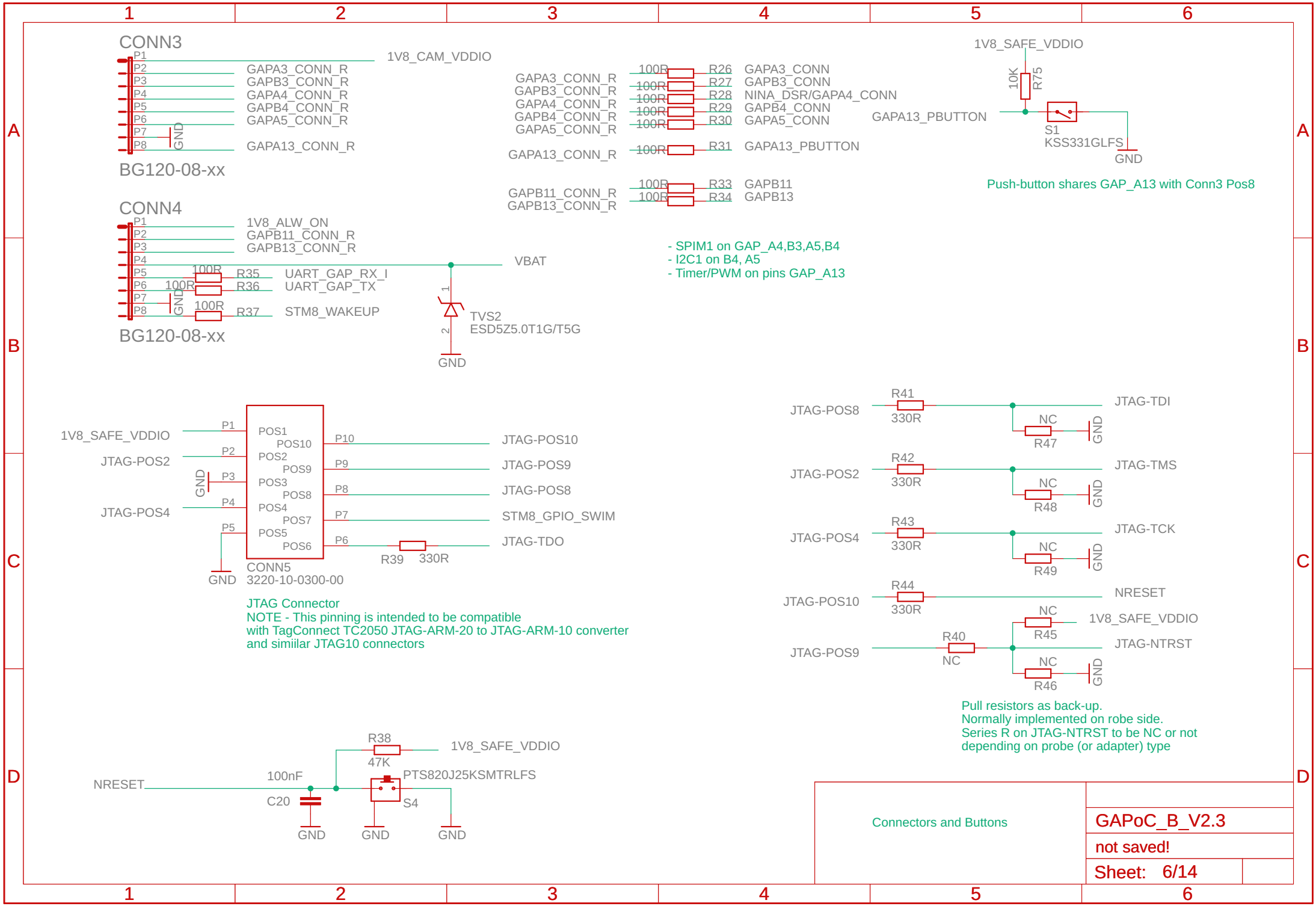
GND GND GND GND GND GND GND GND GND GND GND GND
31 32 33 34 35 36 37 38 39 40 41 42
GND

U8
NINA-B1

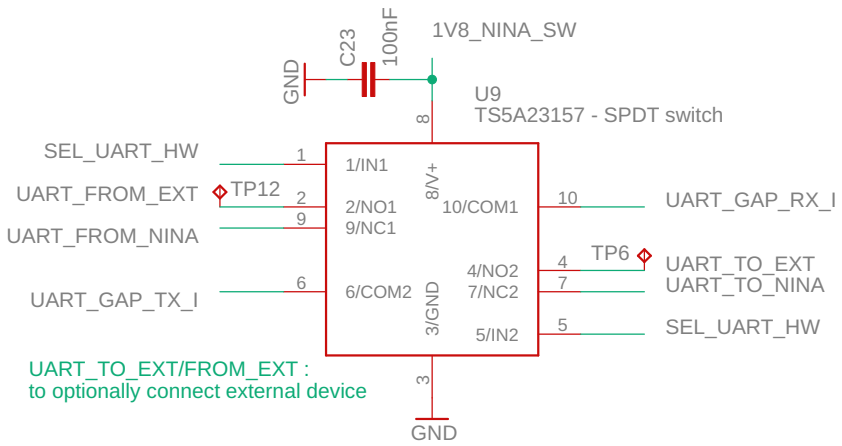
Usage of NINA_DSR (typ. for NINA deep sleep)
exclusive with usage of GAP_A4 on connector
-- in particular, exclusive w/ usage of SPI MISO
of LCD possibly connected to SPI on conn.
Not a big problem as trying to minimie Niina power
(deep sleep) while using power-hungry LCD
wouldn't make much sense...

BLE Module

GAPoC_B_V2.3
not saved!
Sheet: 5/14


CONN3
P1
P2
P3
P4
P5
P6
P7
P8
GND
1V8_CAM_VDDIO
GAPA3_CONN_R
GAPB3_CONN_R
GAPA4_CONN_R
GAPB4_CONN_R
GAPA5_CONN_R
GAPA13_CONN_R
BG120-08-xx
GAPA3_CONN_R
GAPB3_CONN_R
GAPA4_CONN_R
GAPB4_CONN_R
GAPA5_CONN_R
GAPA13_CONN_R
100R
R26
R27
R28
R29
R30
R31
GAPA3_CONN
GAPB3_CONN
NINA_DSR/GAPA4_CONN
GAPB4_CONN
GAPA5_CONN
GAPA13_PBUTTON
1V8_SAFE_VDDIO
10K
R75
S1
KSS331GLFS
GND
Push-button shares GAP_A13 with Conn3 Pos8
CONN4
P1
P2
P3
P4
P5
P6
P7
P8
1V8_ALW_ON
GAPB11_CONN_R
GAPB13_CONN_R
100R
R35
R36
R37
UART_GAP_RX_I
UART_GAP_TX
STM8_WAKEUP
GND
BG120-08-xx
VBAT
TVS2
ESD5Z5.0T1G/T5G
GAPB11_CONN_R
GAPB13_CONN_R
R33
R34
GAPB11
GAPB13
- SPIM1 on GAP_A4,B3,A5,B4
- I2C1 on B4, A5
- Timer/PWM on pins GAP_A13
1V8_SAFE_VDDIO
JTAG-POS2
JTAG-POS4
JTAG-POS10
JTAG-POS9
JTAG-POS8
STM8_GPIO_SWIM
JTAG-TDO
R39
330R
CONN5
3220-10-0300-00
JTAG Connector
NOTE - This pinning is intended to be compatible
with TagConnect TC2050 JTAG-ARM-20 to JTAG-ARM-10 converter
and similar JTAG10 connectors
JTAG-POS8
JTAG-POS2
JTAG-POS4
JTAG-POS10
JTAG-POS9
R41
R42
R43
R44
R40
330R
NC
R47
R48
R49
R45
R46
JTAG-TDI
JTAG-TMS
JTAG-TCK
NRESET
1V8_SAFE_VDDIO
JTAG-NTRST
Pull resistors as back-up.
Normally implemented on robe side.
Series R on JTAG-NTRST to be NC or not
depending on probe (or adapter) type
R38
47K
1V8_SAFE_VDDIO
NRESET
100nF
C20
PTS820J25KSMTRLFS
S4
GND
Connectors and Buttons
GAPoC_B_V2.3
not saved!
Sheet: 6/14

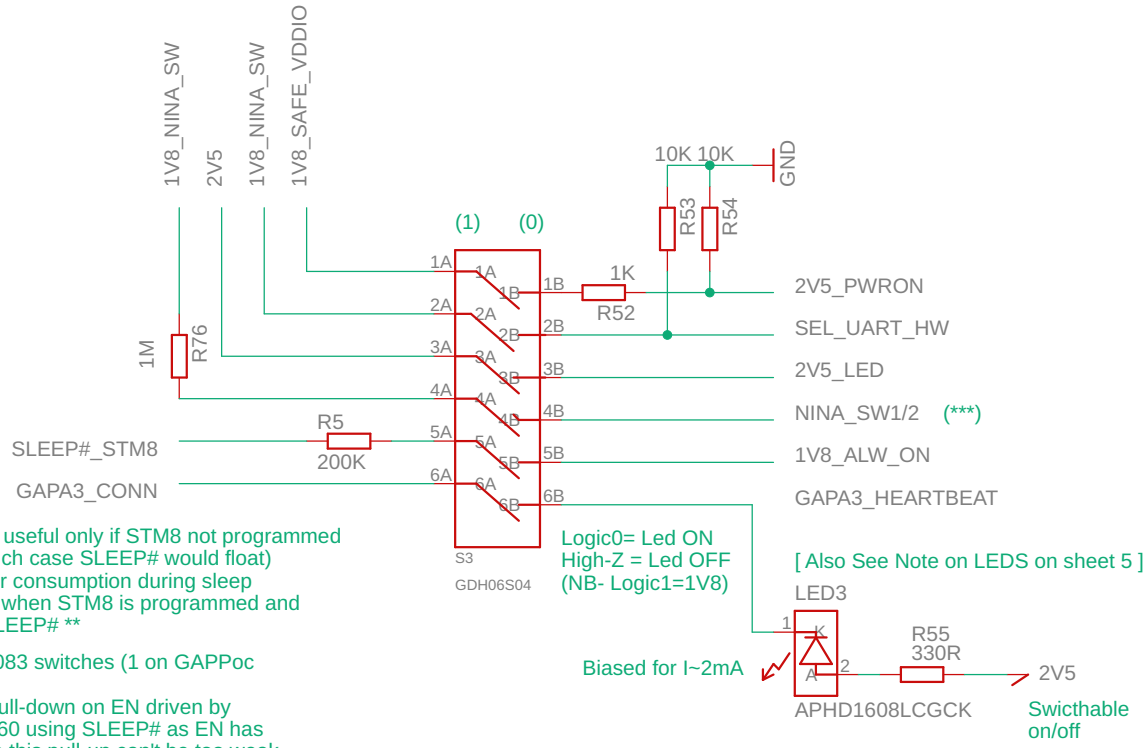
** This could be optimized out **
Dropping UART_TO_EXT, UART_FROM_EXT.
Keeping just UART for Nina (and CONN4)



UART_TO_EXT/FROM_EXT :
to optionally connect external device

Caution:
when 1V8_Nina_Sw is switched off,
GAP8 must drive UART_GAP_TX to Logic0
to avoid excessive power consumption

Open/closed switches :
1: close to provide 2V5 to VQPS pin (Fuse prog.) and to on-board LEDs
2: select if GAP8's UART talks with NINA (open) or with external UART (closed)
3: close to enable status LEDs of NINA & IR sensor (which will draw a few mA)
4: close for nomal boot of Nina
5: close to pull SLEEP# at start-up (required if STM8 not programmed), open to minimize static current
6: close to enable User LED, open to keep A3 available



Pull-up on SLEEP# useful only if STM8 not programmed
/ not present (in which case SLEEP# would float)
Causes ~9uA power consumption during sleep
** Can be removed when STM8 is programmed and
properly controls SLEEP# **

Beware - 2 MIC94083 switches (1 on GAPPoc
and 1 on GAPMod)
have weak (~2M) pull-down on EN driven by
SLEEP# + TPS22960 using SLEEP# as EN has
VIH=1.4V; therefore this pull-up can't be too weak.

*** BEWARE: CLOSE position 4 of DIP switch for proper startup of Nina ***

NINA_SW12 pulled up selects normal boot.
Using large R because same pin becomes LED_G output
after startup (LED not implemented) -- which gets driven
anyway by NINA hence current cons.
Option to eliminiate this extra power consumption by opening switch after startup.

*** BEWARE: CLOSE position 5 of DIP switch of STM8 not programmed / not placed ***
Open once STM8 is programmed, to optimize system deep sleep current

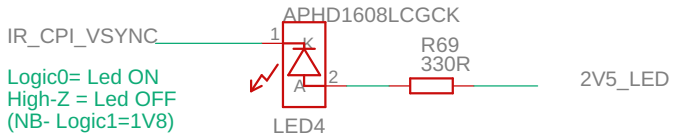
H1 MOUNT-HOLE-2.8
H2 MOUNT-HOLE-2.8
H3 MOUNT-HOLE-2.8
H4 MOUNT-HOLE-2.8

Selection/configuration switches

GAPoC_B_V2.3
not saved!
Sheet: 7/14

Status LED for IR Sensor Bring-up/Debug
Switch off 2V5_LED (cf DIP Switch) to save power
when not required

[Also See Note on LEDS on sheet 5]



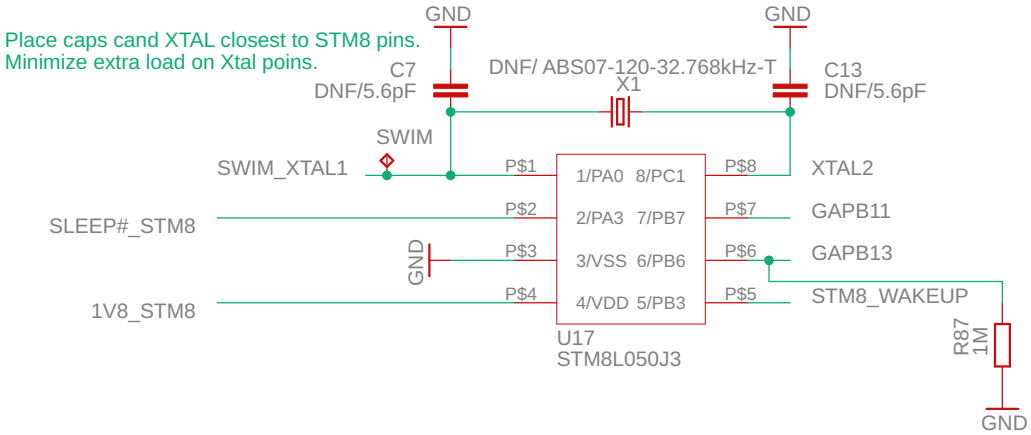
Logic0= Led ON
High-Z = Led OFF
(NB- Logic1=1V8)

Biased for I~2mA

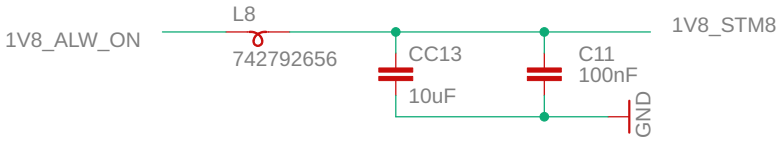
[OPTIONAL -- this provides System DeepSleep/Watchdog + RTC functionality + helps getting to ultra-low system sleep power consumption
** Assembly Option **]

Xtal can be avoided if no RTC required, wake-up from external source only or
if very approximate RTC (hence wake-up) period is acceptable.
STM8 Xtal required only if accurate system RTC functionality is required from STM8.
Else can use LSI of STM8 or just rely on wake-up from GPIO if RTC not needed.
If Xtal is implemented, SWIM must be disconnected from GAP8 after programming
due to pin sharing on STM8.

Place caps cand XTAL closest to STM8 pins.
Minimize extra load on Xtal poins.



Filter supply to STM8 + local bulk cap
to avoid 1V8_STM8 dropping and STM8 rebooting
(brownout reset) when system power is switched
back on at exit of system sleep



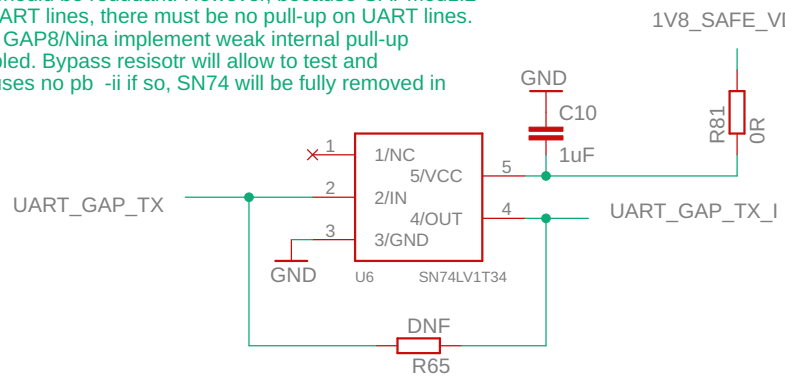
Control of system sleep mode / WatchDog

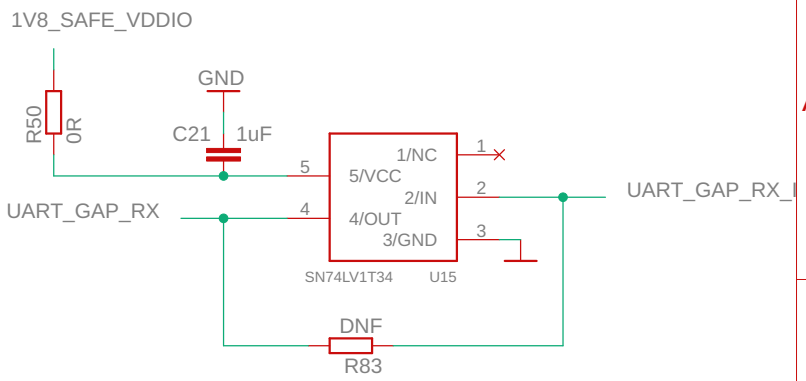
GAPoC_B_V2.3

not saved!

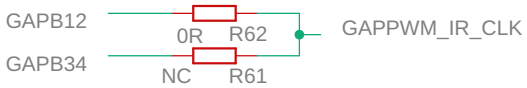
Sheet: 8/14

** Possible optimization **
These 2 SN74LV1T34 were useful when Nina was on 3V.
Since v2.2, Nina is on 1V8 so SN74 should be redudant. However, because GAPMod1.2 employs auto-bidir level shifters on UART lines, there must be no pull-up on UART lines.
For now, still provision SN74, in case GAP8/Nina implement weak internal pull-up on UART I/Os that can't be fully disabled. Bypass resisotr will allow to test and make 100% sure removing SN74 causes no pb -ii if so, SN74 will be fully removed in next revision.

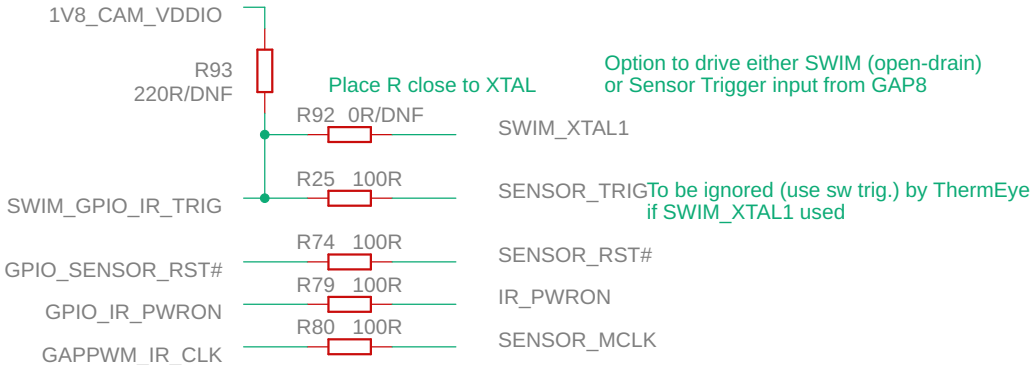




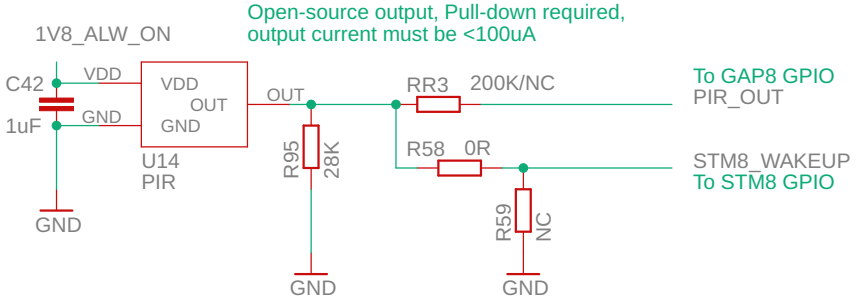
Both I/OSs are Timer/PWM capable



Padframe bug on B34 in CTu1.0/1.1 ==> don't use B34 as PWM, instead use GAPB12 as PWM_IR_CLK
(however keep option to use B34 for when bug fixed as it allows to use IR snesor w/o 1V8 on)



PIR usable to Wake-up GAP8 or STM8



If RR3 implemented then PIR can also wake up GAP8 however in system deep sleep with GAP8 unpowered, will draw 9uA from PIR (if present)

Level Shifter & Misc.

GAPoC_B_V2.3
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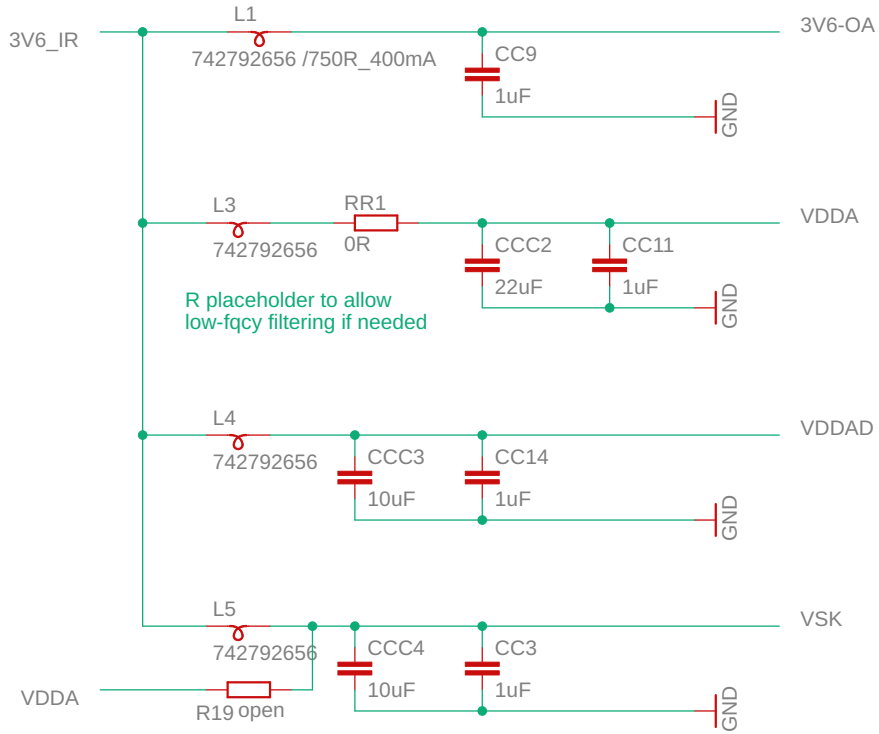

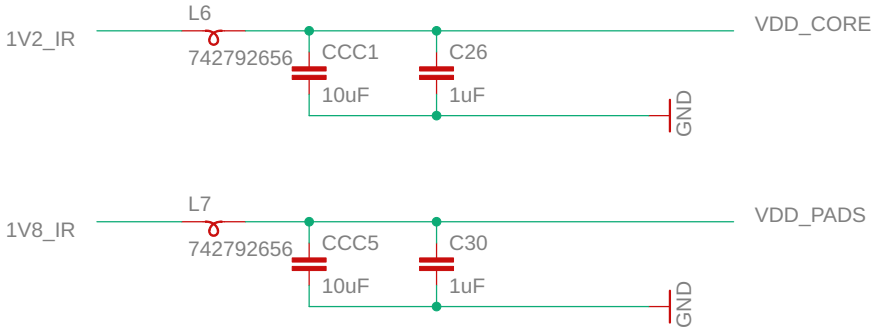

Caps named Cx are 0402 (imp.) dimensions, X5R or X7R dielectric
CCx are 0603
CCCx are 0805
CCCCx are 1206
Ceramic caps effective capacitance decreases vs. nom as DC bias increase
Smaller volume caps are more sensitive to this effect than larger voluame caps.
Cap sizes here were selected to mitigate this effect.

IR Sensor (1/3) Dediated power supply generation and filtering	GAPoC_B_V2.3
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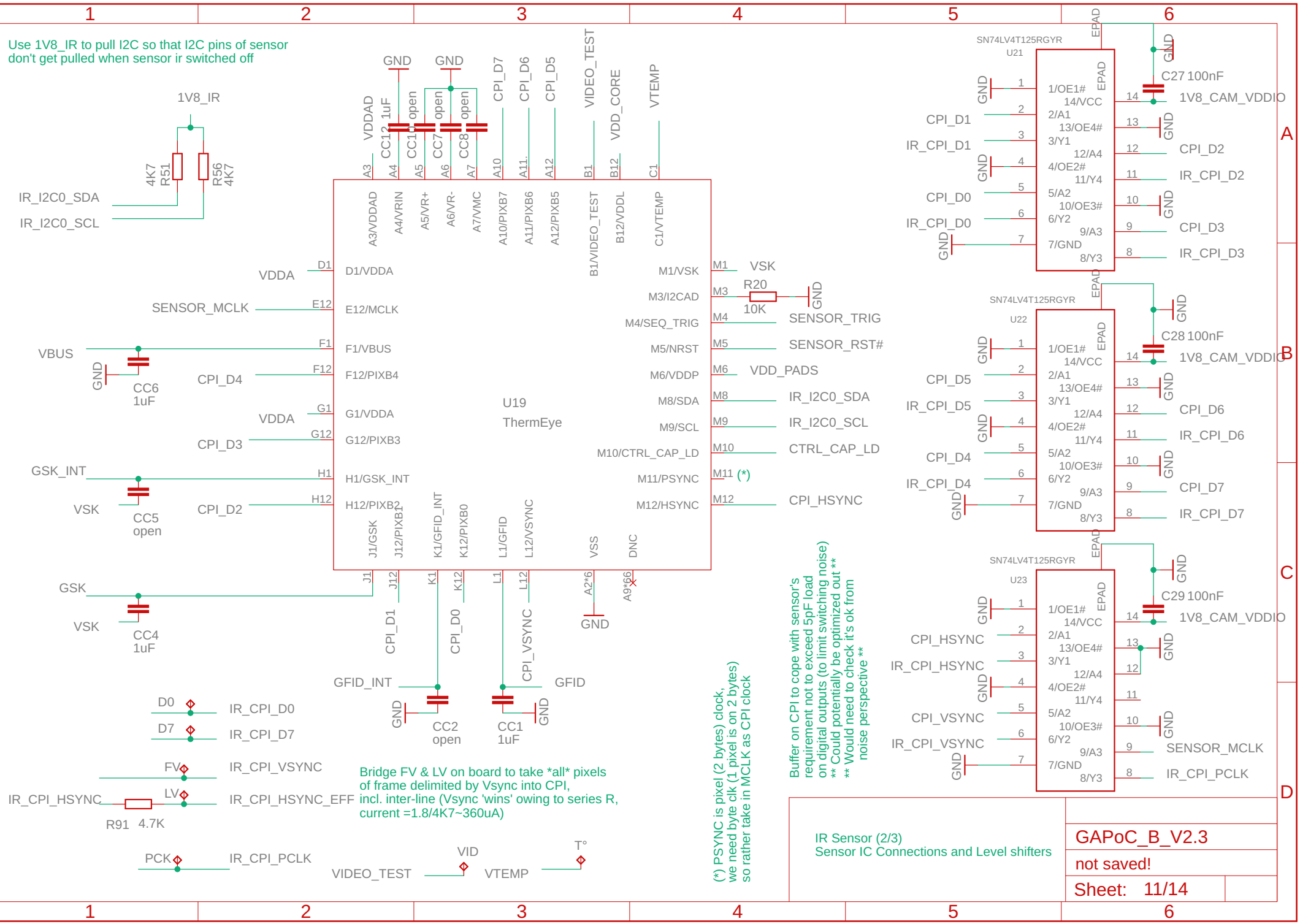
Use 1V8_IR to pull I2C so that I2C pins of sensor don't get pulled when sensor ir switched off
1V8_IR
4K7 R51
R56 4K7
IR_I2C0_SDA
IR_I2C0_SCL
GND
GND
VDDAD
CC12 1uF
CC10 open
CC7 open
CC8 open
CPI_D7
CPI_D6
CPI_D5
VIDEO_TEST
VDD_CORE
VTEMP
A3/VDDAD
A4/VRIN
A5/VR+
A6/VR-
A7/VMC
A10/PIXB7
A11/PIXB6
A12/PIXB5
B1/VIDEO_TEST
B12/VDDL
C1/VTEMP
VDDA
D1/VDDA
SENSOR_MCLK
E12/MCLK
VBUS
F1/VBUS
CPI_D4
F12/PIXB4
VDDA
G1/VDDA
CPI_D3
G12/PIXB3
GSK_INT
H1/GSK_INT
VSK
CC5 open
CPI_D2
H12/PIXB2
U19
ThermEye
M1/VSK
M3/I2CAD
M4/SEQ_TRIG
M5/NRST
M6/VDDP
M8/SDA
M9/SCL
M10/CTRL_CAP_LD
M11/PSYNC
M12/HSYNC
VSK
R20 10K
SENSOR_TRIG
SENSOR_RST#
VDD_PADS
IR_I2C0_SDA
IR_I2C0_SCL
CTRL_CAP_LD
M11 (*)
CPI_HSYNC
J1/GSK
J12/PIXB1
K1/GFID_INT
K12/PIXB0
L1/GFID
L12/VSYNC
VSS
DNC
GSK
VSK
CC4 1uF
CPI_D1
CPI_D0
CPI_VSYNC
GFID_INT
GFID
CC2 open
CC1 1uF
GND
D0
IR_CPI_D0
D7
IR_CPI_D7
FV
IR_CPI_VSYNC
IR_CPI_HSYNC
LV
IR_CPI_HSYNC_EFF
R91 4.7K
PCK
IR_CPI_PCLK
VIDEO_TEST
VID
VTEMP
T°
Bridge FV & LV on board to take *all* pixels of frame delimited by Vsync into CPI, incl. inter-line (Vsync 'wins' owing to series R, current =1.8/4K7~360uA)
(*) PSYNC is pixel (2 bytes) clock, we need byte clk (1 pixel is on 2 bytes) so rather take in MCLK as CPI clock
Buffer on CPI to cope with sensor's requirement not to exceed 5pF load on digital outputs (to limit switching noise)
** Could potentially be optimized out **
** Would need to check it's ok from noise perspective **
SN74LV4T125RGYR
U21
1/OE1#
14/VCC
2/A1
13/OE4#
3/Y1
12/A4
4/OE2#
11/Y4
5/A2
10/OE3#
6/Y2
9/A3
7/GND
8/Y3
EPAD
C27 100nF
1V8_CAM_VDDIO
CPI_D1
IR_CPI_D1
CPI_D0
IR_CPI_D0
CPI_D2
IR_CPI_D2
CPI_D3
IR_CPI_D3
SN74LV4T125RGYR
U22
C28 100nF
1V8_CAM_VDDIO
CPI_D5
IR_CPI_D5
CPI_D4
IR_CPI_D4
CPI_D6
IR_CPI_D6
CPI_D7
IR_CPI_D7
SN74LV4T125RGYR
U23
C29 100nF
1V8_CAM_VDDIO
CPI_HSYNC
IR_CPI_HSYNC
CPI_VSYNC
IR_CPI_VSYNC
SENSOR_MCLK
IR_CPI_PCLK
IR Sensor (2/3)
Sensor IC Connections and Level shifters
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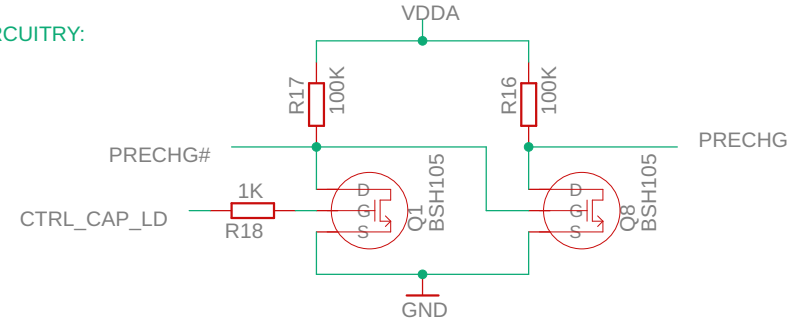
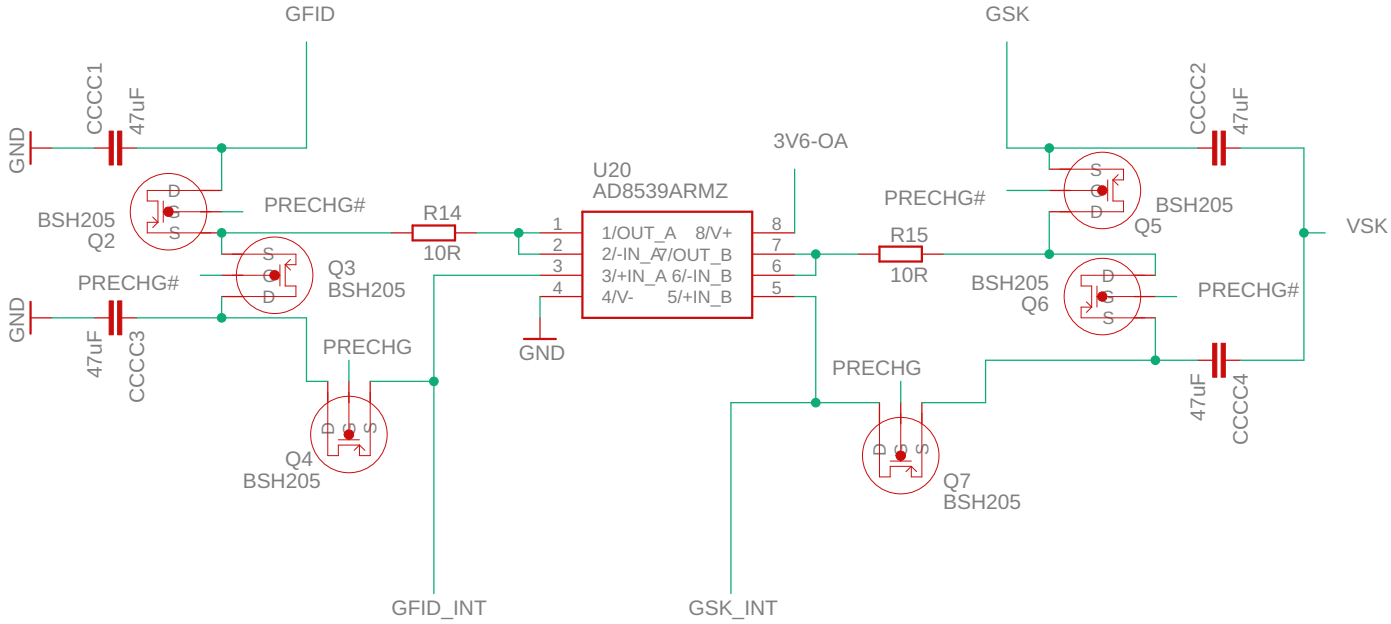
GENERATION OF PRECHARGE SIGNALS FOR BOOST CIRCUITRY:



GENERATION OF GFID AND GSK USING "TIME BOOST" :



IR Sensor (3/3)
Biasing with time boost

GAPoC_B_V2.3

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